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Question Paper Code : 86650

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Fourth Semester

Electrical and Electronics Engineering

EC 1261 A — DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering)

(Regulations 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Simplify : $xy + x'z + yz$.

2. Draw the circuit of the function $F = \Sigma(0, 6)$ with NAND gates.

3. Give the characteristic equation and state diagram of JK flip-flop.

4. What is lockout? How it is avoided?

5. What is meant by transition table?

6. Name the types of hazards.

7. What is the difference between PROM and EPROM?

8. What are the advantages of CMOS?

9. List the different types of 'operators' supported by VHDL.

10. The 'module' is the basic building block of VHDL. What are the different modelling techniques used to describe a module?

PART B — (5 × 16 = 80 marks)

11. (a) With the use of Maps, Find the simplest form in SOP of the function $F = f.g$, where f and g are given by

$f = wxy' + y'z + w'yz' + x'yz'$

$g = (w + x + y' + z')(x' + y' + z)(w' + y + z')$. (16)

Or

(b) (i) Design BCD to Excess — 3 code converter using BPA. (8)

(ii) Design a 3 bit magnitude comparator using gates. (8)

12. (a) (i) Realize SR flip-flop using NOR gates and explain its operation. (8)

(ii) Convert a SR flip-flop into JR flip-flop. (8)

Or

(b) A sequential circuit with 2D FFs A and B and input X and output Y is specified by the following next state and output equations. (16)

$A(t+1) = AX + BX$

$B(t+1) = A'X$

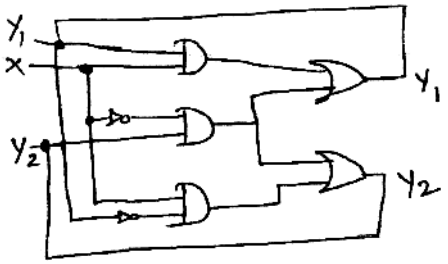
$Y = (A + B)X'$

(i) Draw the logic diagram of the circuit.

(ii) Derive the state table.

(iii) Derive the state diagram.

13. (a) Consider the following asynchronous sequential circuit and draw maps and transition table, and state table. (16)



Or

(b) Illustrate the analysis procedure of asynchronous sequential circuit with an example. (16)

14. (a) (i) Implement a $1\text{M} \times 4$ RAM using 512 K × 4 RAM. (8)

(ii) Explain in details about TTL with open Collector output configuration. (8)

Or

(b) (i) Implement the following functions using PLA

$F_1 = \Sigma\, m\,(1,\ 2,\ 4,\ 6);\ F_2\ \Sigma\, m\,(0,\ 1, 6,\ 7);\ F_3 = \Sigma\, m\,(2,\ 6)$. (8)

(ii) Demonstrate the CMOS logic circuit configuration and characteristics in details. (8)

15. (a) (i) Briefly discuss the different data types supported in VHDL. (6)

(ii) Write the HDL description of the circuit specified by the following Boolean functions:

$x = A + BC + B'D$

$y = B'C + BC'D'$

Use continuous assignment statements. (10)

Or

(b) (i) Briefly discuss the use of 'Packages' in VHDL. (6)

(ii) Write an HDL code that implements an 8:1 multiplexer. (10)

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